



Agilent Technologies

PCI Express Protocol Test – Part 1

July 30th 2003

presented by:

Roland Scherzinger

Agenda

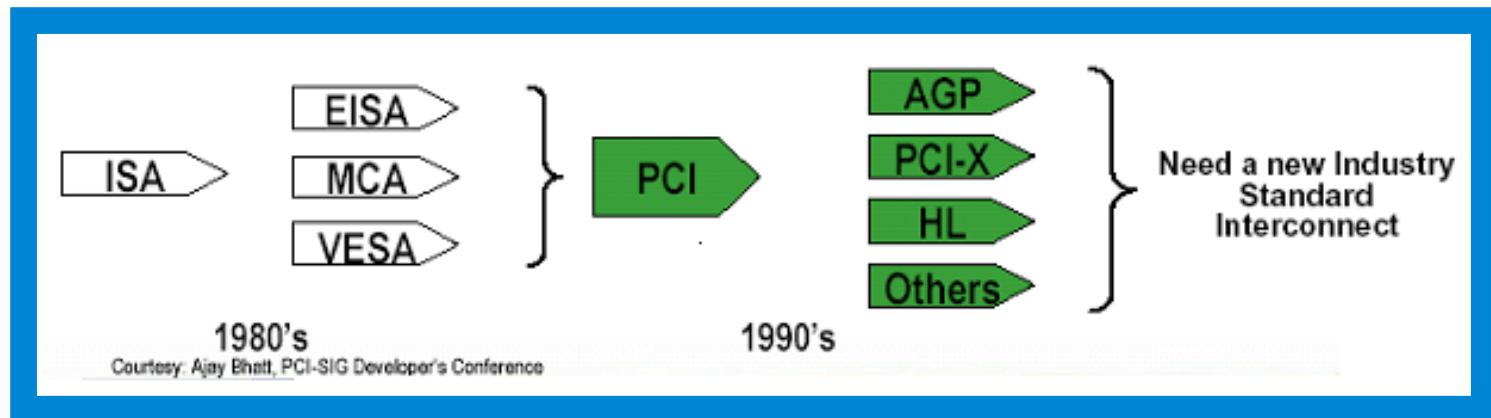
→ Introduction

- Turn on a new PCI Express Device
- Validation of PCI Express Devices and Systems
- Checking for PCI Express Compliance
- Demo

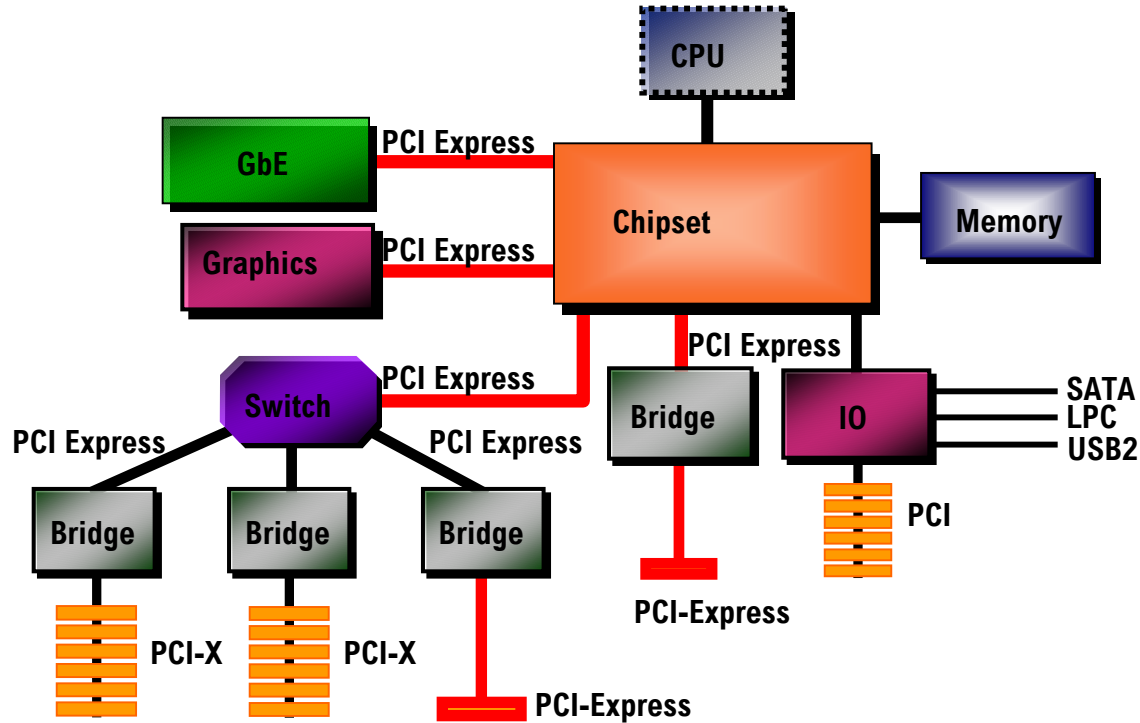


Why PCI Express?

- Mountains of data = demand for greater bandwidth - key market drivers include 3D games, image processing, HDTV encoding.
- Parallel speed limit - Physical limitations of parallel bus technology
- Fragmentation increases cost – New standard needed to achieve economies of scale for diverging requirements for different application/market segments (AGP, PCI, PCI-X, HubLink etc)



New Measurement Requirements



Compliance Testing

- Pass/Fail information
- Pushbutton Tests

Physical Layer Tests

- TDR measurements
- Physical layer protocol test
- BERT
- Eye Diagram

Protocol Analysis

- Find protocol failures
- Validate traffic flow
- Message error identification
- Packet error identification
- Measure performance (Utilization, Throughput, Overhead, etc.)

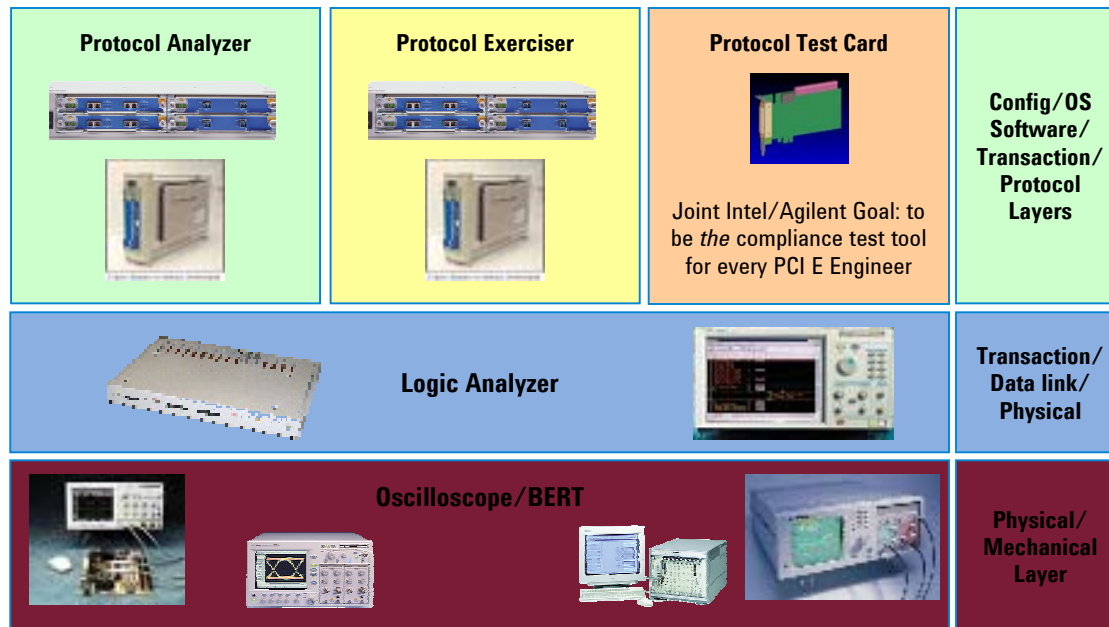
Protocol Exercising

- Protocol Variation Testing
- Multi-Port Switch Testing
- Load simulation
- End-to-end path testing
- Throughput validation
- Error response testing



Agilent Test Tools for PCI Express

Agilent's integrated platform for PCI Express test series supports the move to serial system I/O for the computer industry and protects customer investment.



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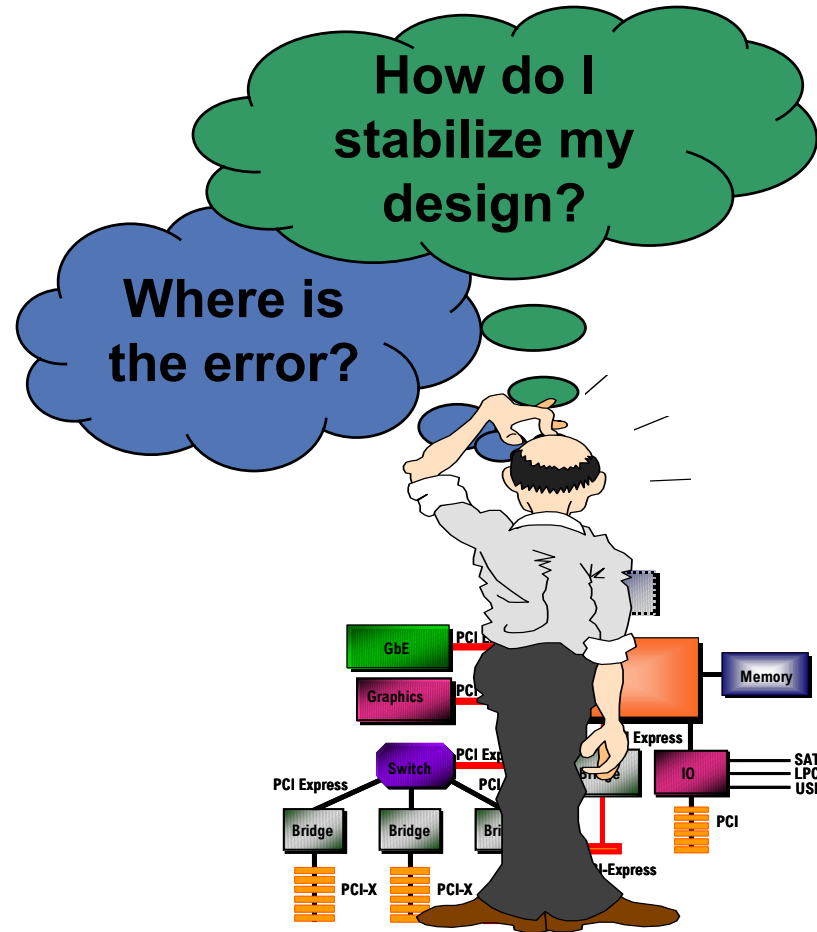
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Bring Up & Debug Tasks / Needs



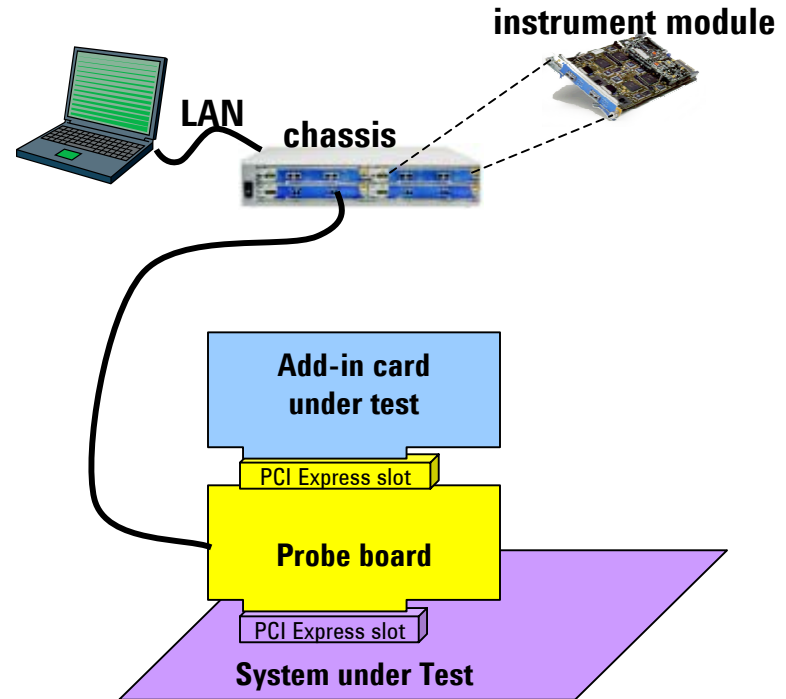
- Ensure basic functionality and stability of the new design as quickly as possible
- Get fast insight to potential problems!
- Make debugging predictable and repeatable!



Bring Up & Debug Test Solution



- Protocol Analyzer
 - **Dynamic Trigger Conditions** for simplified triggering on sophisticated transactions
 - GUI with trigger, search and filter capabilities to intuitively interpret PCI Express traffic
 - Root cause and performance analysis
- Protocol Exerciser
 - as stimulus to complement Protocol Analyzer



Protocol Analyzer - Graphical User Interface



Serial Protocol Analyzer

File Hardware Display Help

Layer 1

Dir.	Timestamp	Type	Requester ID	Tag	Length	Address			
←	01:23.456	Memory Read Request	0xF123	170	1	5603328			
←	01:23.456	Memory Read Request	0xF123	170	1	5603328			
⇒	01:23.456	Memory Read Request	0xF123	170	1	5603328			
←	01:23.456	Completion							
←	01:23.456	I/O Read Request	0xF123	170		5603328			
←	01:23.456	3							
Reserved	Fmt	Type	Reserved	Traffic Class	Reserved	TLP Digest	TLP poisoned	Attr	Reser
0	3DW header, no data	3	0	0	0	Absent	false	0	0
⇒	01:23.456	Memory Write Request	0xF123	170	1				
⇒	01:23.456	I/O Write Request	FE	205	8	15935102			
Reserved	Fmt	Type	Reserved	Traffic Class	Reserved	TLP Digest	TLP poisoned		
0	3DW header, with data	I/O write Request	0	0	0	Absent	false		
⇒	01:23.456	Completion with data			1				
Reserved	Fmt	Type	Reserved	Traffic Class	Reserved	TLP Digest	TLP pois		

Memory Read; Adr=0x3000; Len=0x100; Status=OK
Memory Read; Adr=0x103040; Len=0x1000; Status=FAIL
IO Read; Bus=7, Device=3, Function=0

statusBar1

Callouts:

- expand/collapse individual packets to get more details
- color coded transaction types allow easy recognition of various types of traffic
- tabular view with configurable columns
- packets with errors are highlighted with special background (e.g. red)
- context sensitive field decoding
- second view pane provides alternate view of traffic (e.g. textual, statistical, etc.)
- tooltips for each field provide more detailed info as needed

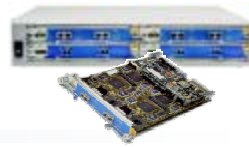


Agenda

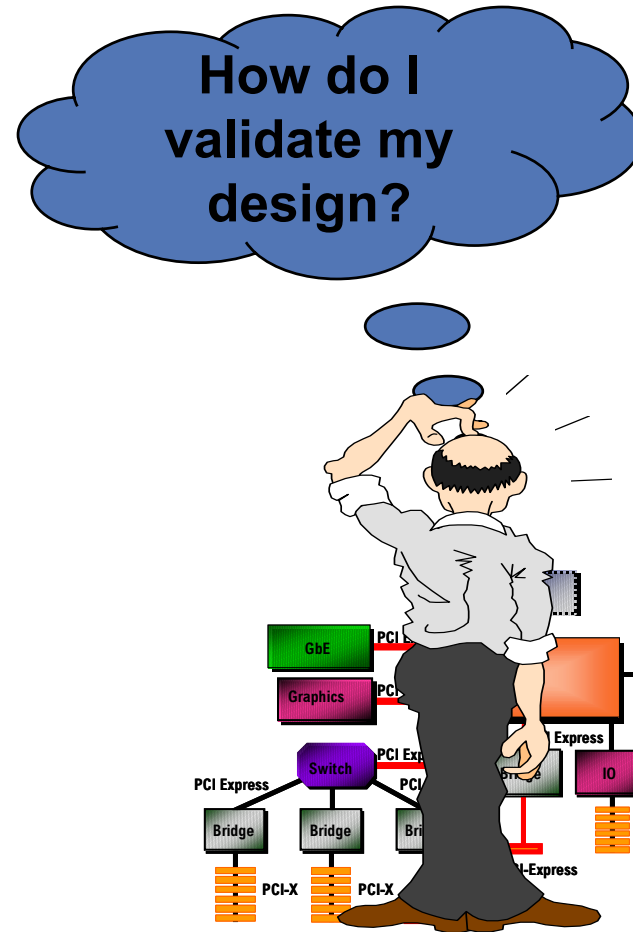
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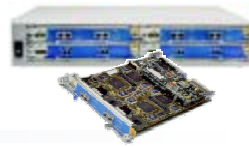
Validation Requirements



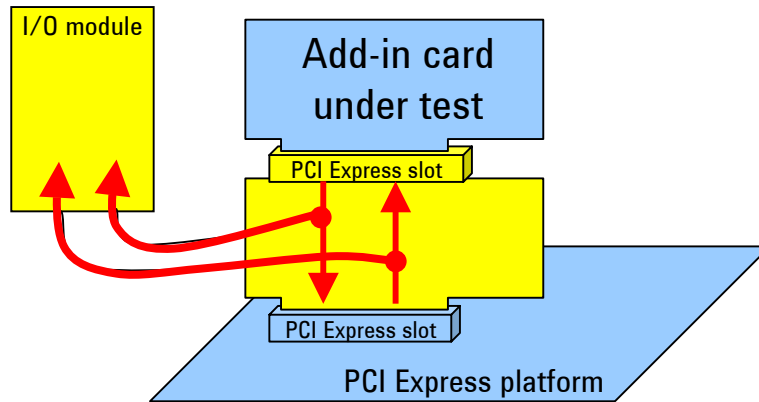
- Robustness of the new design
 - Test all transients of the link statemachine
 - Test protocol and data integrity under maximum bandwidth conditions
 - Test all data paths concurrently
 - Expose the new design to as many as possible protocol variations
 - Make sure, errors are handled correctly



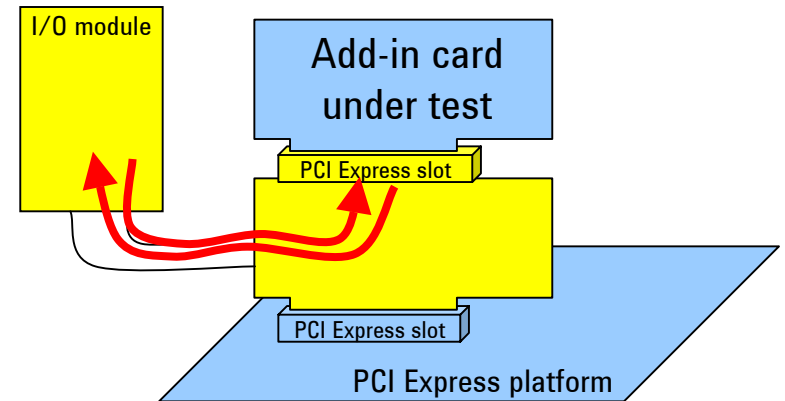
One setup - three use cases



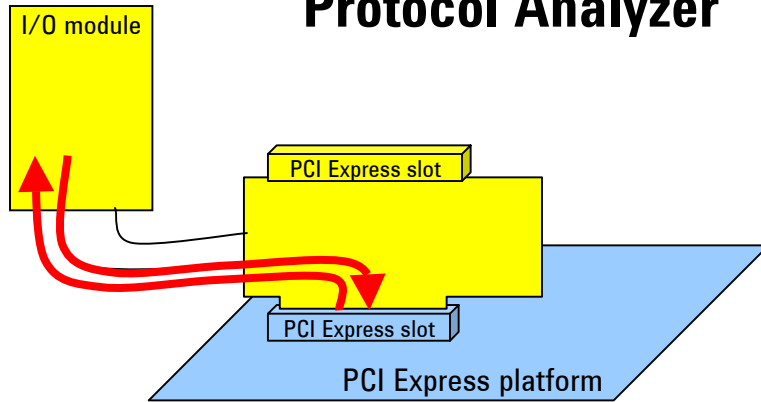
(all software controlled - no change of physical setup)



Protocol Analyzer



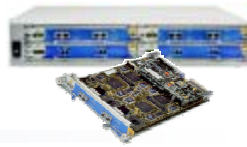
Exerciser for add-in card



Exerciser for platform



Protocol Exerciser Features



- Supports x1, x2, x4, x8 link widths at full bandwidth
- Exerciser can act as an end-node (for platform testing) or act as a root-complex (for add-in card testing). Exerciser can also emulate the config space of a switch.
- Physical connection using x8, x4 or x1 probe board
- Add-in cards up to 16x can be plugged into the probe board (link width limited to 8x)
- Exerciser can interactively generate and respond to arbitrary transactions
- Payload can be algorithmic or memory-based (memory size 2M)
- Various error insertion capabilities on physical, data link and transaction layers
- Programmable through external interface (100 BaseT LAN) or in-system (config space accesses on PCI-Express link under test)
- C++, TCL and COM programming interfaces

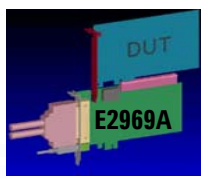


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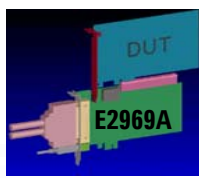
Compliance Test Needs



- Pass the plugfest tests
- Check if the BIOS is capable to configure any type of add-in card
- Check for correct implementation of the config space
- Does the data link layer correctly transfer the data over the link
- Error checking, etc ...

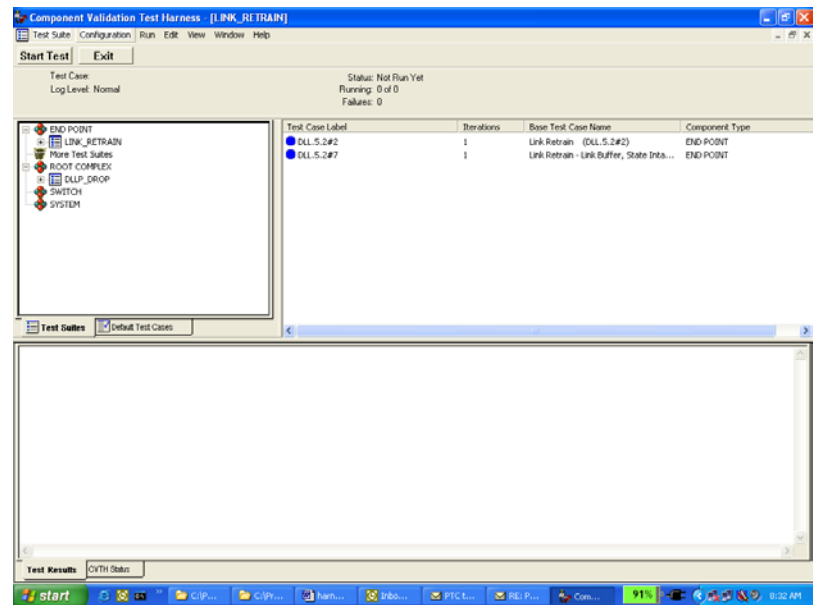


Compliance Test Solution



- PCI Express add-in card (normal PCI Express form factor) for x1
- Supports add-in cards with up to x16 Lane Width
- Agilent/Intel collaboration (<http://www.agilent.com/about/newsroom/presrel/2003/10apr2003a.html>)
- Automated pre-canned compliance tests for the Transaction Layer and the Data Link Layer
- Known endpoint, switch and topology simulation mode
- Tests power management and configuration space
- Field upgradeable FPGA-based card
- Connection to protocol analyzer
- Card controlled via PCI Express or via an external host over USB 2.0

Agilent E2969A Protocol Test Card



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- **Demo**



Demo

- Using the Exerciser, perform a memory read request with the parameters:
 - Address: 0x00000001:0000ead0
 - Length: 0x10 Dwords
 - TC: 0x1
 - LASTDWBE: 0xC
- Analyze the traffic with the protocol analyzer



Exerciser Programming Example

```
void main(void)
{
    pExerciser = SetupExerciserConnection(&portHandle);

    // Use the SendImmediate capability to transmit a memory read request

    // Set some Si (send immediate) Packet properties
    pExerciser->SiDefaultSet(portHandle);

    pExerciser->SiReqSet(portHandle, PCIE_PKT_FMT, 1);
    pExerciser->SiReqSet(portHandle, PCIE_PKT_TYPE, 0);
    pExerciser->SiReqSet(portHandle, PCIE_PKT_LEN, 0x10);
    pExerciser->SiReqSet(portHandle, PCIE_PKT_TC, 0x1);
    pExerciser->SiReqSet(portHandle, PCIE_PKT_LASTDWBE, 0xc);
    pExerciser->SiReqSet(portHandle, PCIE_PKT_MEM64_ADDRLO, 0xead0);
    pExerciser->SiReqSet(portHandle, PCIE_PKT_MEM64_ADDRHI, 0x1);

    // Send the TLP
    pExerciser->SiSend(portHandle);
}
```



Trigger Setup

The screenshot displays the 'TriggerWindow' application interface. The window title is 'TriggerWindow' and it has a 'File' menu. The main area is divided into two sections: configuration on the left and a 'State Machine Visualisation' on the right.

Configuration Section:

- State:** A dropdown menu is set to 'S1', with 'Add' and 'Remove' buttons.
- IF Section:** Includes a checkbox for 'NOT', a text field containing 'TLP', an action field containing 'Store,Trigger', and a 'Goto State' dropdown set to 'S1'.
- ELSE IF Section:** Includes a checkbox for 'NOT', a text field containing 'DLLP Ack', an action field containing 'Store', and a 'Goto State' dropdown set to 'S2'.
- ELSE Section:** Includes an action field containing 'Store' and a 'Goto State' dropdown set to 'S1'.
- Buttons at the bottom of the configuration area are 'Remove ELSE IF' and 'Add ELSE IF'.

State Machine Visualisation:

- Shows two states: 'S1' (a blue circle) and 'S2' (a white circle).
- Transitions: An arrow from S1 to S2 is labeled 'Store'. A self-loop on S1 is labeled 'Store,Trigger'. A self-loop on S2 is labeled 'No Action'.
- Checkboxes at the bottom: 'Show Conditions' (unchecked) and 'Show Actions' (checked).
- 'Ok' and 'Cancel' buttons are at the bottom right.



View the Data

The screenshot shows the Serial Protocol Analyzer interface. The main window displays a list of captured packets. Packet 21 is selected and highlighted in blue. The details for packet 21 are shown below the list:

Dir.	Packet Nr	Timestamp	Type	CRC					
←	21	0:00:32.687							
Fmt		Type	Traffic Class	TLP Digest	TLP poisoned	Attr	Length	Requester ID	Tag
4DW header, no data		Memory Read Request	001b	Absent	false	00b	0x000A		0x15
Last DW BE	First DW BE	Address							
1100b	1111b	0x000000010000EAD1							

Other packets visible in the list include:

- Packet 20: UpdateFC-Cpl, Virtual Channel 0, HdrFC 0x06, DataFC 0x0018, CRC 0xAD34
- Packet 22: Nak, AckNack_Seq_Num 0x0008, CRC 0xAD34
- Packet 23: Memory Read Request, Traffic Class 001b, TLP Digest Absent, TLP poisoned false, Attr 00b, Length 0x000A, Requester ID, Tag 0x15, Address 0x000000010000EAD0
- Packet 24: UpdateFC-P, Virtual Channel 0, HdrFC 0x03, DataFC 0x0008, CRC 0xAD34
- Packet 25: UpdateFC-P, Virtual Channel 0, HdrFC 0x03, DataFC 0x0008, CRC 0xAD34
- Packet 26: UpdateFC-P, Virtual Channel 0, HdrFC 0x03, DataFC 0x0008, CRC 0xAD34



View the Data

Serial Protocol Analyzer

File Capture Display Window Help

Layer 3

Dir.	Packet Nr	Timestamp	Type	Tag	Length	Address				
←	0	0:00:32.687	Memory Read Request	0x15	0x000A	0x000000010000EAD1				
Fmt		Type		Traffic Class	TLP Digest	TLP poisoned	Attr	Length	Requester ID	Tag
4DW header, no data		Memory Read Request		001b	Absent	false	00b	0x000A	61731	0x15
Last DW BE	First DW BE	Address								
1100b	1111b	0x000000010000EAD1								
←	1	0:00:33.473	Memory Read Request	0x15	0x000A	0x000000010000EAD0				
Fmt		Type		Traffic Class	TLP Digest	TLP poisoned	Attr	Length	Bus Number	
4DW header, no data		Memory Read Request		001b	Absent	false	00b	0x000A	0xF1	
Device Number	Function Number	Tag	Last DW BE	First DW BE	Address					
0x04	0x03	0x15	1100b	1111b	0x000000010000EAD0					
⇒	2	0:00:42.630	Completion with data	0x15	0x000A					
Fmt		Type		Traffic Class	TLP Digest	TLP poisoned	Attr	Length	Completer ID	
3DW header, with data		Completion with data		001b	Absent	false	00b	0x000A	0xF130	
Completion Status		BCM	Byte Count	Bus Number	Device Number	Function Number	Tag	Lower Address		
Successful Completion		0b	0x0028	0xF1	0x04	0x03	0x15	0x50		
Payload										
0xC0000000C0000001C0000002C0000003C0000004C0000005C0000006C0000007C0000008C0000009										

0:00:32.687: MemRead, Length: 320, Requester ID: 61731, Address: 0x000000010000EAD1
 0:00:33.473: MemRead, Length: 320, Requester ID: 61731, Address: 0x000000010000EAD0, Length: 320, Requester ID: 61731

statusBar1



Summary

Debug/Bring up Easier and quicker

- Patented “Dynamic Trigger Conditions” for simplified triggering on sophisticated transactions
- First PCI Express x8 Protocol Analyzer and Exerciser combination for optimized design bring up and debug

Target customers:

Software developers and hardware designers who bring up and debug PCI Express designs in the entire computer industry such as drivers, BIOS, add in cards, motherboards, chips and systems.

Validation

Increasing test coverage in less test time

- Full speed PCI Express x8 and x4 server and chipset validation solution
- First Protocol Exerciser for PCI Express x8 on market by shipping in August 2003

Target customers:

Engineers and lab managers in R&D, validation and QA labs validating PCI Express chipsets, boards, systems and platforms in the entire computer industry.

Compliance test

Cost effective push button solution for compliance testing

- First PCI Express compliance test solution with link into debug environment
- Complements Intel's PDK for optimal compliance testing

Target customers:

Software developers and hardware designers who need to prove PCI Express compliance of their PCI Express designs.



Example Configuration

E2960A-B08: Bring-Up & Debug solution for PCI Express 8x

