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PCI Express Protocol Test – Part 1

July 30th 2003

presented by:

Roland Scherzinger

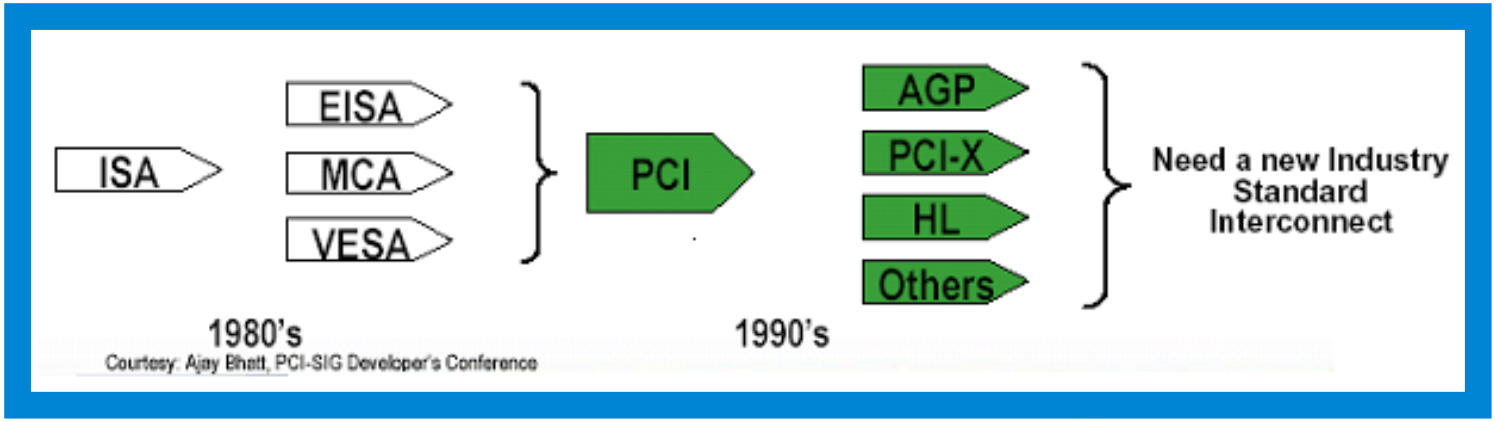
Agenda

→Introduction

- Turn on a new PCI Express Device
- Validation of PCI Express Devices and Systems
- Checking for PCI Express Compliance
- Demo

Why PCI Express?

- Mountains of data = demand for greater bandwidth - key market drivers include 3D games, image processing, HDTV encoding.
- Parallel speed limit - Physical limitations of parallel bus technology
- Fragmentation increases cost – New standard needed to achieve economies of scale for diverging requirements for different application/market segments (AGP, PCI, PCI-X, HubLink etc)



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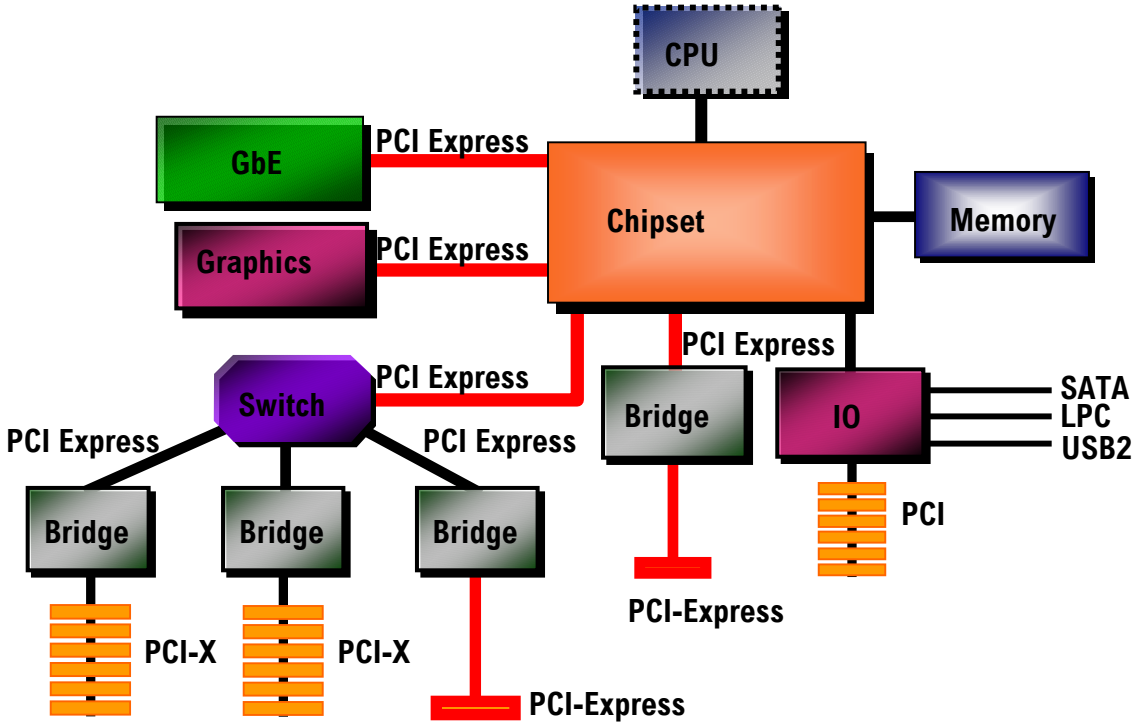
New Measurement Requirements



Protocol Analysis

- Find protocol failures
- Validate traffic flow
- Message error identification
- Packet error identification
- Measure performance (Utilization, Throughput, Overhead, etc.)

Compliance Testing

- Pass/Fail information
- Pushbutton Tests

Physical Layer Tests

- TDR measurements
- Physical layer protocol test
- BERT
- Eye Diagram

Protocol Exercising

- Protocol Variation Testing
- Multi-Port Switch Testing
- Load simulation
- End-to-end path testing
- Throughput validation
- Error response testing

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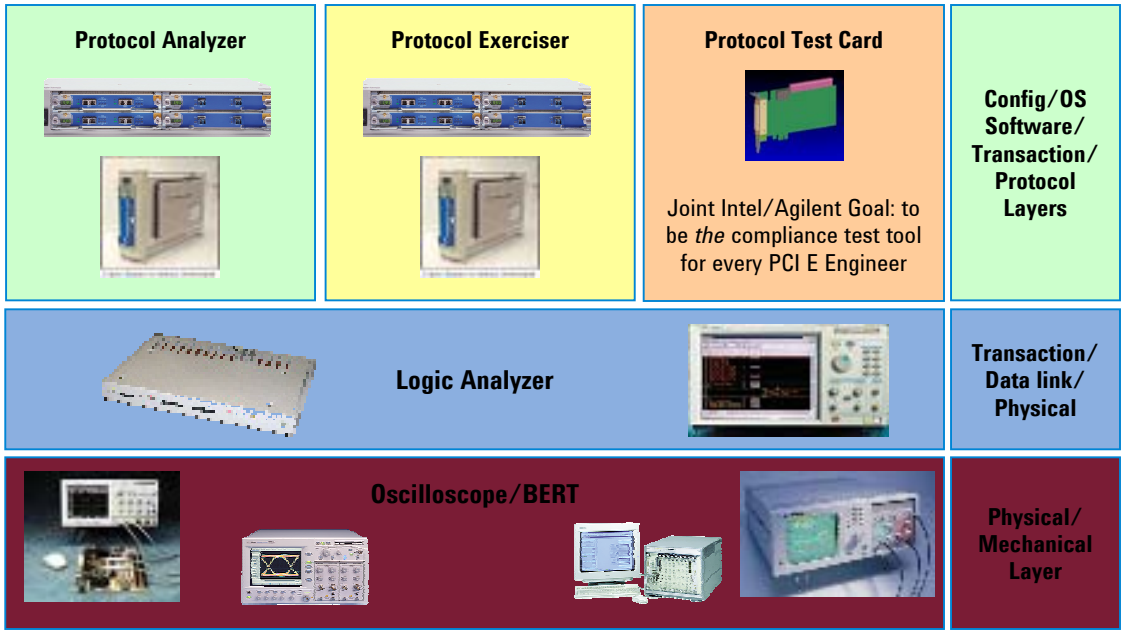
Agilent Test Tools for PCI Express

Agilent's integrated platform for PCI Express test series supports the move to serial system I/O for the computer industry and protects customer investment.



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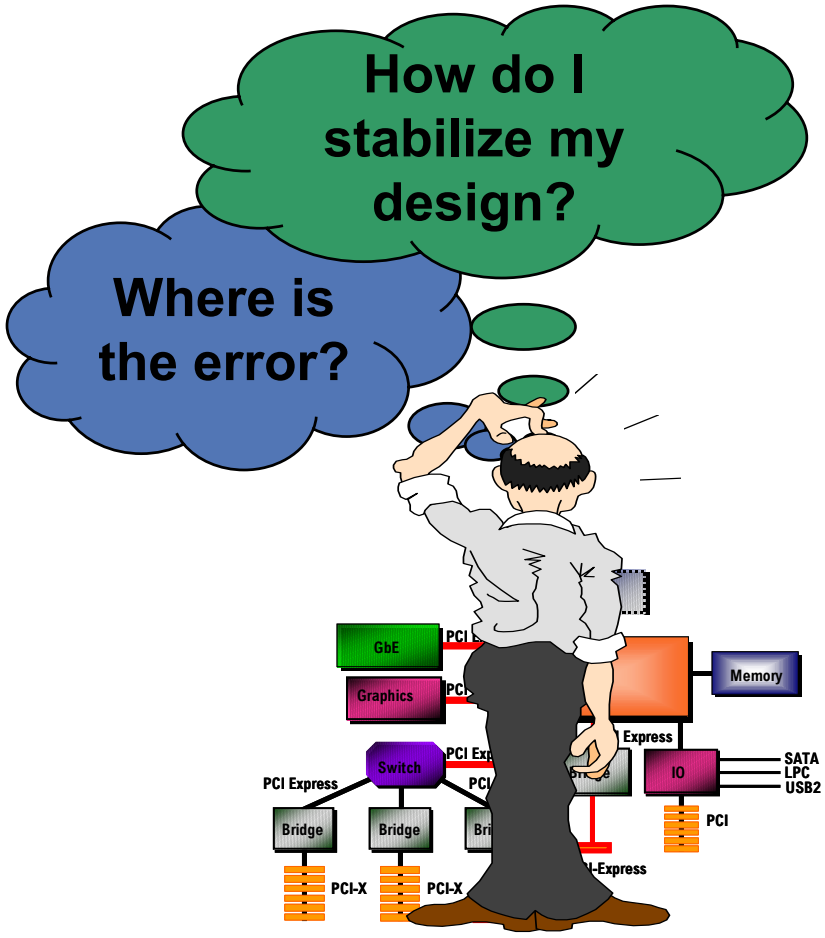
Bring Up & Debug Tasks / Needs

- Ensure basic functionality and stability of the new design as quickly as possible
- Get fast insight to potential problems!
- Make debugging predictable and repeatable!



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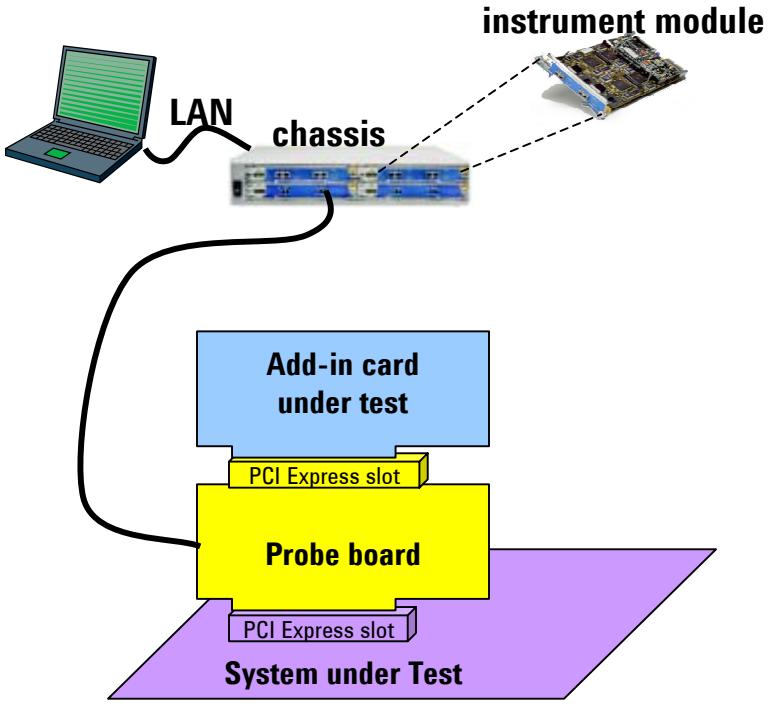
Bring Up & Debug Test Solution

- Protocol Analyzer
  - **Dynamic Trigger Conditions** for simplified triggering on sophisticated transactions
  - GUI with trigger, search and filter capabilities to intuitively interpret PCI Express traffic
  - Root cause and performance analysis
- Protocol Exerciser
  - as stimulus to complement Protocol Analyzer



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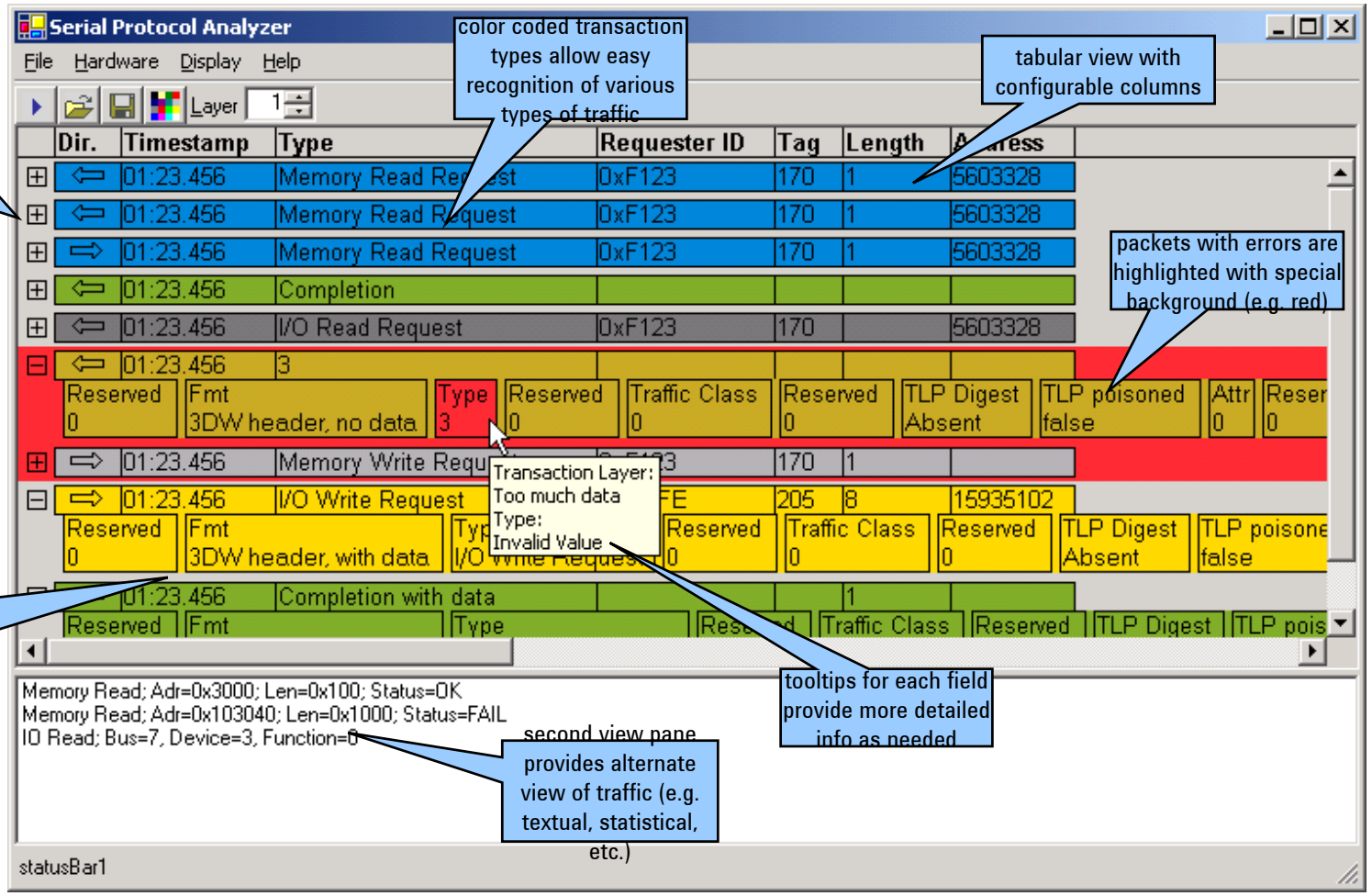
Protocol Analyzer - Graphical User Interface



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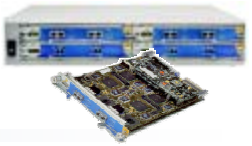
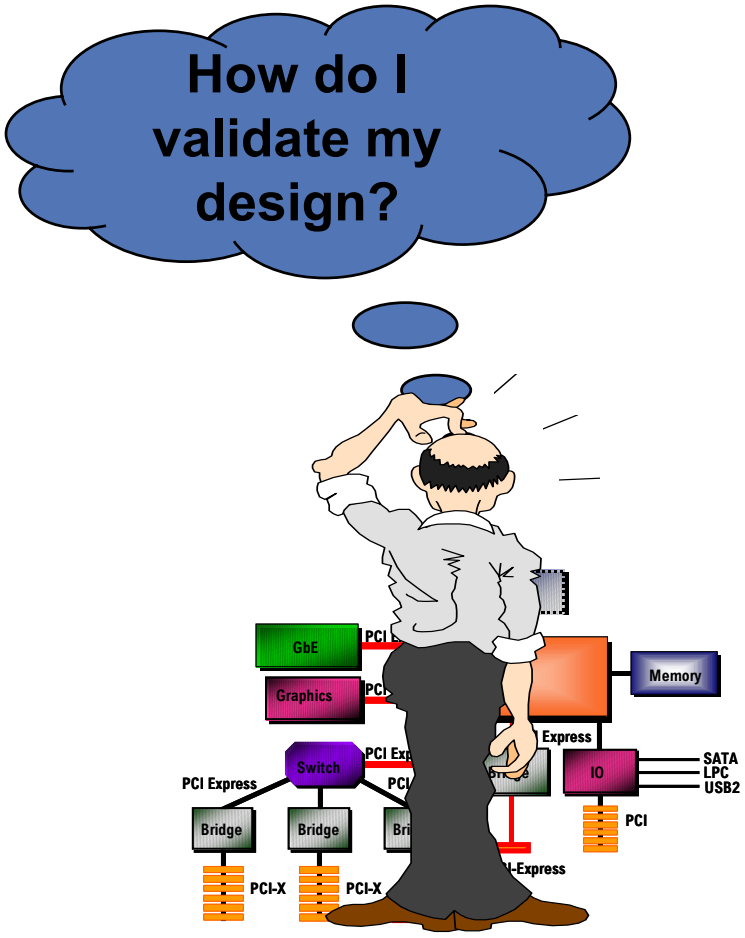
Validation Requirements



- Robustness of the new design
  - Test all transients of the link statemachine
  - Test protocol and data integrity under maximum bandwidth conditions
  - Test all data paths concurrently
  - Expose the new design to as many as possible protocol variations
  - Make sure, errors are handled correctly



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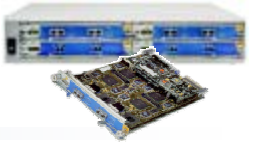
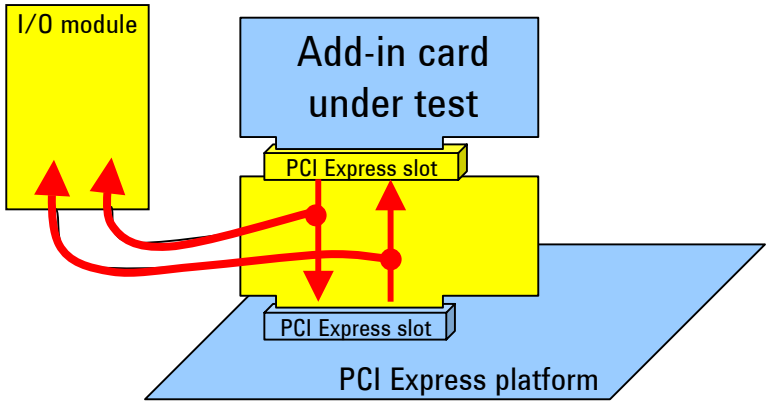
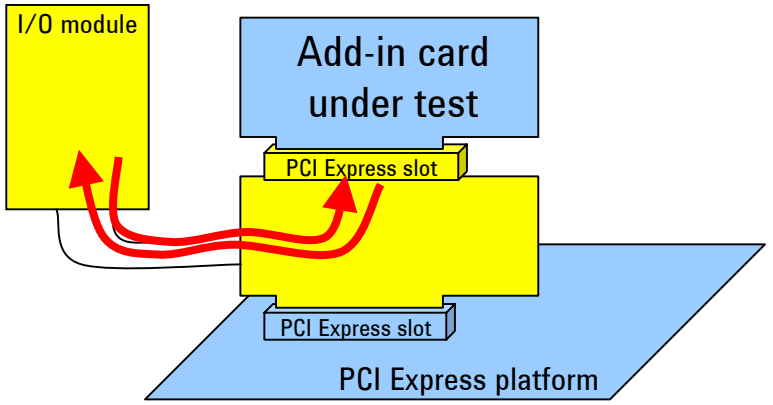
One setup - three use cases



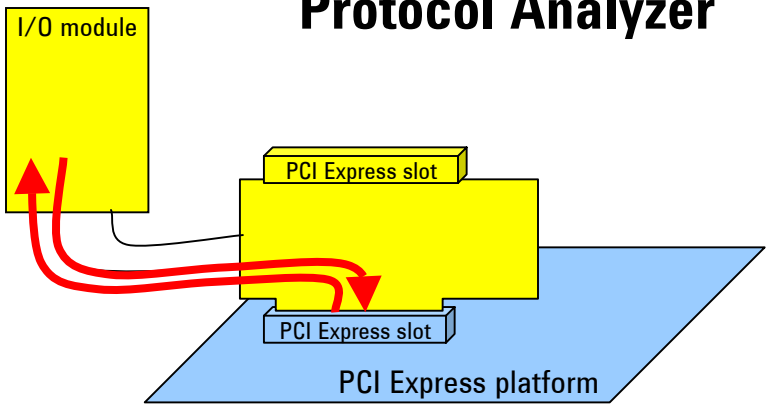
(all software controlled - no change of physical setup)



Protocol Analyzer



Exerciser for add-in card



Exerciser for platform

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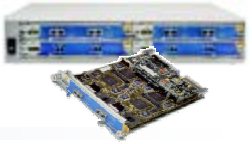
Protocol Exerciser Features



- Supports x1, x2, x4, x8 link widths at full bandwidth
- Exerciser can act as an end-node (for platform testing) or act as a root-complex (for add-in card testing). Exerciser can also emulate the config space of a switch.
- Physical connection using x8, x4 or x1 probe board
- Add-in cards up to 16x can be plugged into the probe board (link width limited to 8x)
- Exerciser can interactively generate and respond to arbitrary transactions
- Payload can be algorithmic or memory-based (memory size 2M)
- Various error insertion capabilities on physical, data link and transaction layers
- Programmable through external interface (100 BaseT LAN) or in-system (config space accesses on PCI-Express link under test)
- C++, TCL and COM programming interfaces

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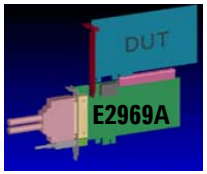
→**Checking for PCI Express Compliance**

- Demo

Compliance Test Needs



- Pass the plugfest tests
- Check if the BIOS is capable to configure any type of add-in card
- Check for correct implementation of the config space
- Does the data link layer correctly transfer the data over the link
- Error checking, etc …

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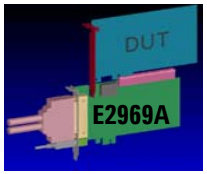
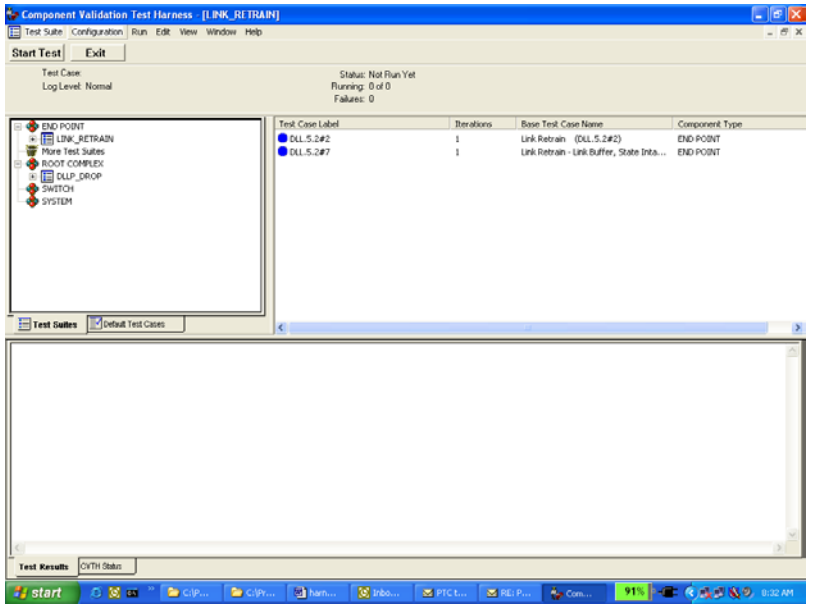
Compliance Test Solution



- PCI Express add-in card (normal PCI Express form factor) for x1
- Supports add-in cards with up to x16 Lane Width
- Agilent/Intel collaboration (http://www.agilent.com/about/newsroom/presrel/2003/10apr2003a.html)
- Automated pre-canned compliance tests for the Transaction Layer and the Data Link Layer
- Known endpoint, switch and topology simulation mode
- Tests power management and configuration space
- Field upgradeable FPGA-based card
- Connection to protocol analyzer
- Card controlled via PCI Express or via an external host over USB 2.0

Agilent E2969A Protocol Test Card



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→**Demo**

Demo

- Using the Exerciser, perform a memory read request with the parameters:
  - Address: 0x00000001:0000ead0
  - Length: 0x10 Dwords
  - TC: 0x1
  - LASTDWBE: 0xC
- Analyze the traffic with the protocol analyzer

Exerciser Programming Example

```
void main(void)
{
    pExerciser = SetupExerciserConnection(&portHandle);

    // Use the SendImmediate capability to transmit a memory read request

    // Set some Si (send immediate) Packet properties
    pExerciser->SiDefaultSet(portHandle);

    pExerciser->SiReqSet(portHandle, PCIE_PKT_FMT, 1);
    pExerciser->SiReqSet(portHandle, PCIE_PKT_TYPE, 0);
    pExerciser->SiReqSet(portHandle, PCIE_PKT_LEN, 0x10);
    pExerciser->SiReqSet(portHandle, PCIE_PKT_TC, 0x1);
    pExerciser->SiReqSet(portHandle, PCIE_PKT_LASTDWBE, 0xc);
    pExerciser->SiReqSet(portHandle, PCIE_PKT_MEM64_ADDRLO, 0xead0);
    pExerciser->SiReqSet(portHandle, PCIE_PKT_MEM64_ADDRHI, 0x1);

    // Send the TLP
    pExerciser->SiSend(portHandle);

}
```

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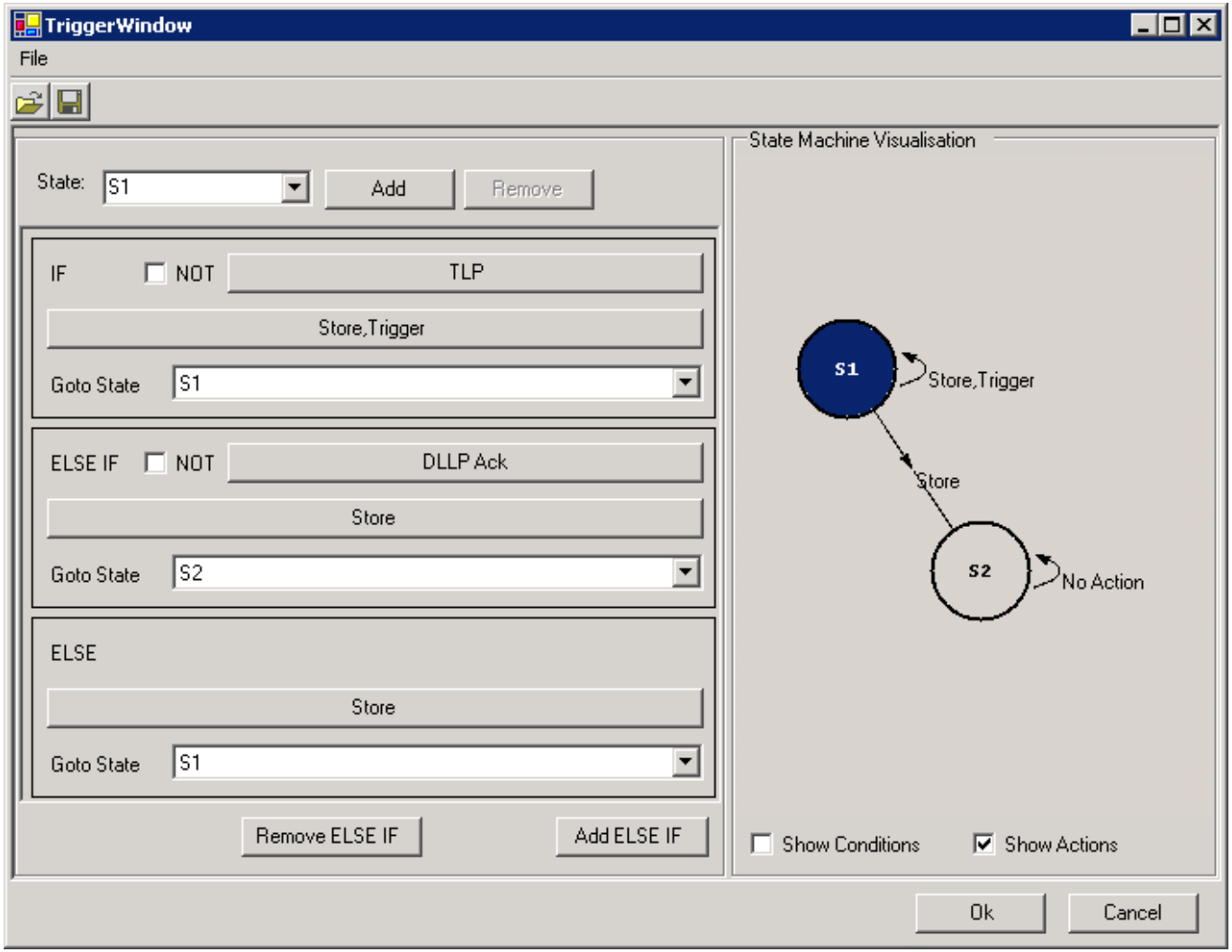
Trigger Setup



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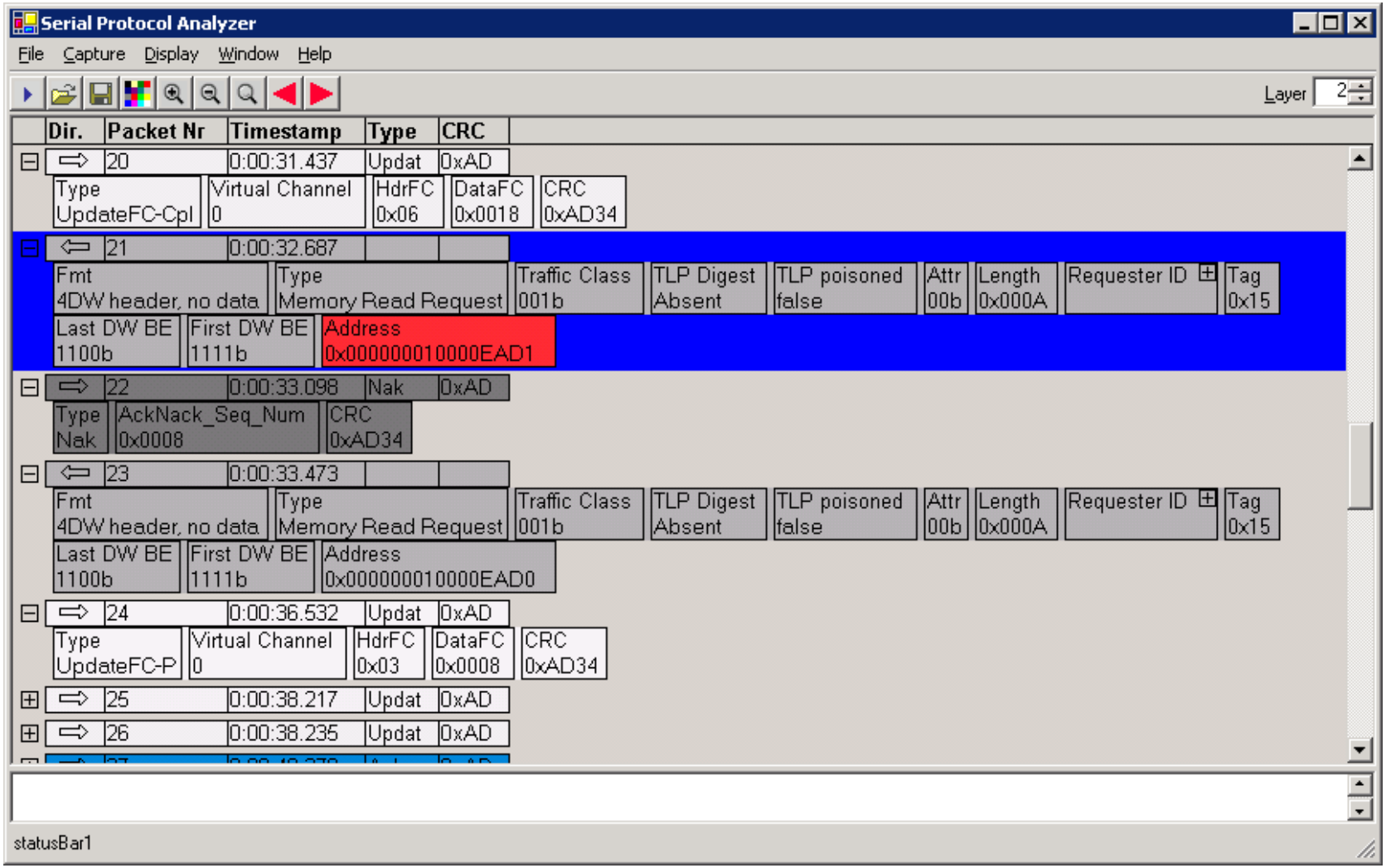
View the Data



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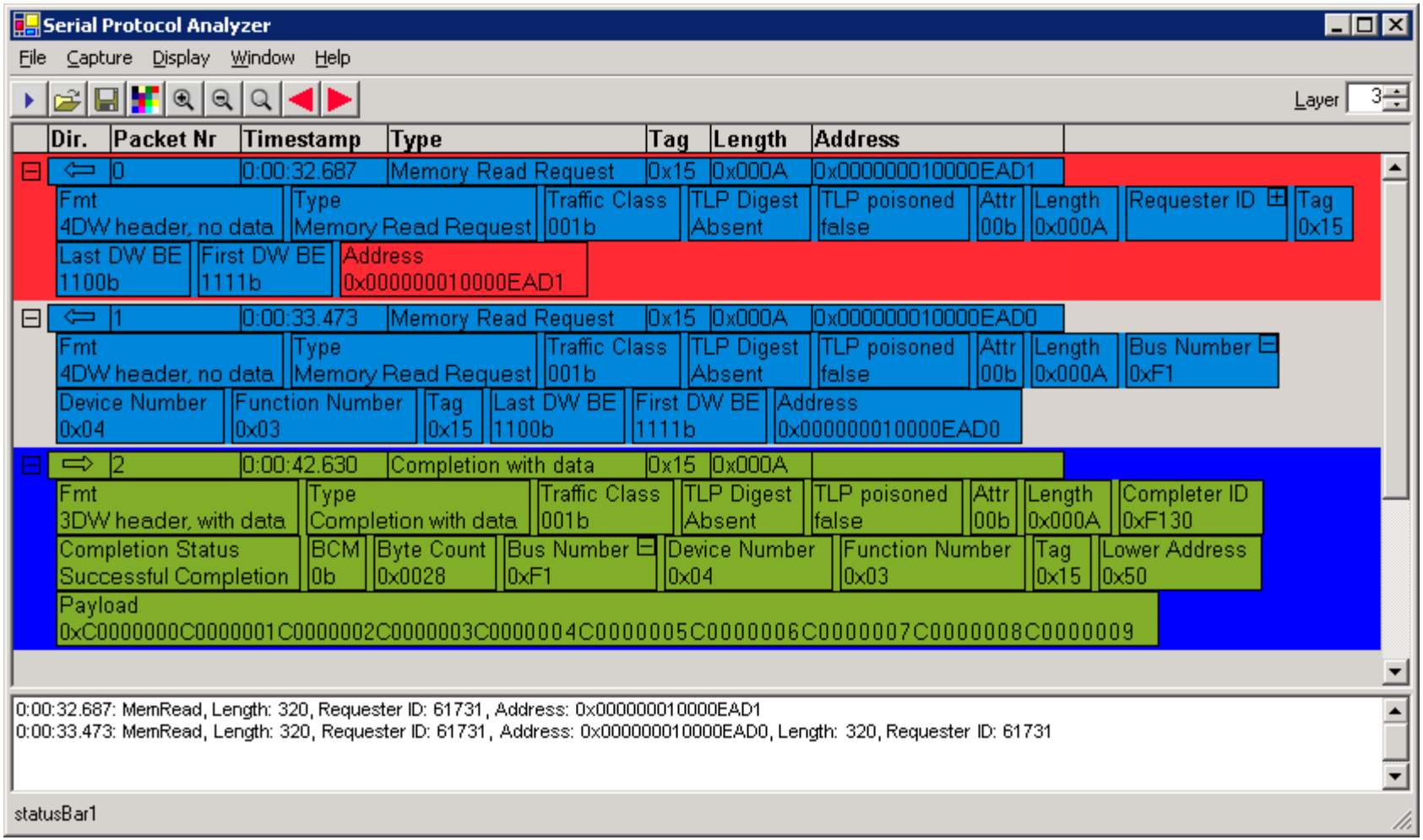

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Summary

Debug/Bring up
Easier and quicker

- Patented "Dynamic Trigger Conditions" for simplified triggering on sophisticated transactions
- First PCI Express x8 Protocol Analyzer and Exerciser combination for optimized design bring up and debug

Target customers:
Software developers and hardware designers who bring up and debug PCI Express designs in the entire computer industry such as drivers, BIOS, add in cards, motherboards, chips and systems.

Validation
Increasing test coverage in less test time

- Full speed PCI Express x8 and x4 server and chipset validation solution
- First Protocol Exerciser for PCI Express x8 on market by shipping in August 2003

Target customers:
Engineers and lab managers in R&D, validation and QA labs validating PCI Express chipsets, boards, systems and platforms in the entire computer industry.

Compliance test
Cost effective push button solution for compliance testing

- First PCI Express compliance test solution with link into debug environment
- Complements Intel's PDK for optimal compliance testing

Target customers:
Software developers and hardware designers who need to prove PCI Express compliance of their PCI Express designs.

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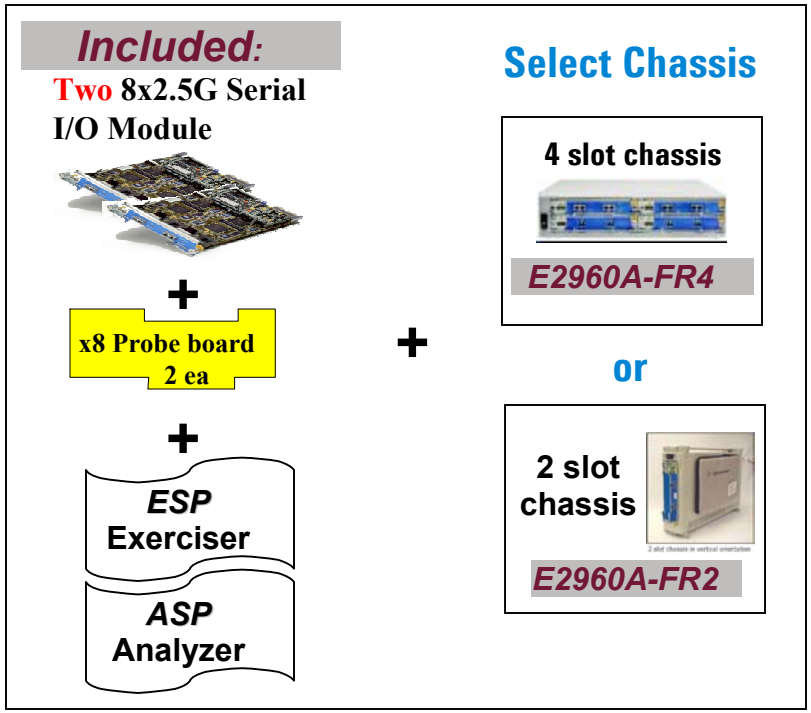
Example Configuration

E2960A-B08: Bring-Up & Debug solution for PCI Express 8x



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